

Pubblico Concorso, per titoli ed esami, per la copertura a tempo indeterminato di n. 5 posti di Collaboratore Tecnico Professionale - Ingegnere Elettronico, Cat. D, indetto con Determinazione Dirigenziale n. 8239 del 05.11.2019 e con Determinazione Dirigenziale n. 195 del 19.01.2021

VERBALE N. 4

Il giorno 15.09.2022, alle ore 09,00, si è riunita presso la sede del Centro Professionale Lavoro Formazione, in Selargius, Via Piero della Francesca snc, la Commissione Esaminatrice del Pubblico Concorso di cui all'oggetto, nominata con Determinazione Dirigenziale n. 2125 del 08.07.2022, e composta come di seguito specificato:

Presidente

Ing. Galisai Marco, Dirigente Ingegnere dell'ARES;

Componente nominato dalla Direzione Aziendale

Ing. Rossi Michele, Collaboratore Tecnico Professionale - Ingegnere Elettronico, Cat. D, dell'AUSL Toscana Nord Ovest;

Componente nominato dal Collegio di Direzione

Ing. Testoni Giampiero, Dirigente Ingegnere dell'ARES;

Segretario

Dott. Madeddu Andrea, Collaboratore Amministrativo Professionale, Cat. D, dell'ARES;

Il Presidente, constatata la regolare costituzione della Commissione e la legalità dell'adunanza, essendo presenti tutti i componenti, dichiara aperta la seduta.

La Commissione prende atto preliminarmente che i membri aggiunti, presa visione dell'elenco dei partecipanti, hanno dichiarato che non sussistono situazioni di incompatibilità né ex art. 35 del D. Lgs. n. 165/2001, né con i candidati, così come contemplato dagli artt. 51 e 52 del c.p.c., come da note allegate agli atti del concorso.

La Commissione si è riunita per procedere allo svolgimento della prova orale così come previsto dagli articoli 9 e 16 del D.P.R. n. 220/2001.

La prova orale verterà sulle materie relative alla disciplina a concorso, nonché sui compiti connessi alla funzione da conferire.

Nell'ambito della prova orale verrà accertata, altresì, la conoscenza dell'uso delle apparecchiature e delle applicazioni informatiche più diffuse e della lingua inglese.

I criteri di valutazione della prova orale terranno conto della padronanza dell'argomento, della capacità di discussione e chiarezza espositiva e di comunicazione.

Il superamento della prova orale è subordinato al raggiungimento di una valutazione di sufficienza, espressa in termini numerici, di almeno 14/20.

Conseguono l'idoneità i candidati che abbiano superato, con giudizio positivo, il colloquio per l'accertamento della conoscenza della lingua inglese e delle apparecchiature e applicazioni informatiche più diffuse.

Saranno, pertanto, sottoposte a ciascun candidato:

- n. 1 domanda relativa al profilo professionale a concorso;
- n. 1 domanda di informatica;
- n. 1 testo in lingua inglese da leggere e tradurre.

Vengono predisposte dalla Commissione le seguenti n. 14 domande al fine di consentire anche all'ultimo candidato la possibilità di scelta, che, inserite in buste chiuse, verranno estratte direttamente dai singoli partecipanti:









N.	DOMANDA
1	A. Descrivere il funzionamento del comando Ping B. Cos'è il Cardiology Information System (CIS) e quali sono le sue principali funzionalità?
2	A. Descrivere una piattaforma di virtualizzazione B. Descrivere il funzionamento del comando Traceroute
3	A. Cos'è un PACS e quali sono le sue principali funzionalità? B. Cos'è un data center?
4	A. Descrivere i modelli ISO-OSI e TCP/IP a confronto B. Cos'è un sistema RIS e quali sono le sue principali funzionalità?
5	A. Cos'è l'Order Entry in un sistema informativo sanitario? B. Descrivere il livello 1 del modello ISO-OSI (Layer Fisico)
6	A. Cos'è un Profilo di Integrazione IHE? B. Descrivere le topologie di reti più comuni
7	B. Descrivere il livello 2 del modello ISO-OSI (Layer Data Link) B. Cosa è il sistema FSE?
8	A. Come sono organizzate le informazioni in un database relazionale? B. Descrivere il livello 3 del modello ISO-OSI (Layer Network)
9	A. Quali caratteristiche deve avere una Postazione di Refertazione della Radiologia? B. Cosa significa il termine "Open Source"?
10	A. Descrivere il livello 4 del modello ISO-OSI (Layer di Trasporto) B. Che cos'è il Dicom Conformance Statement?
11	A. Cosa si intende per classificazione di un data center TIER I ? B. Descrivere in cosa consiste un dominio di collisione
12	A. Cosa significa DICOM e cosa rappresenta? B. Cosa si intende per classificazione di un data center TIER II ?
13	A. Descrivere in cosa consiste un dominio di broadcast B. Cosa significa HL7 e cosa rappresenta?
14	A. Cos'è il Sistema di Conservazione? B. Descrivere la funzione del protocollo IP (Internet Protocol)

Per quanto concerne la prova relativa all'accertamento dell'uso delle apparecchiature e delle applicazioni informatiche, il Dott. Deplano Emiliano, componente aggiunto della Commissione, stabilisce, in accordo con i membri di quest'ultima, di predisporre una prova unica per tutti i candidati presenti consistente nella verifica della conoscenza dell'uso delle predette apparecchiature ed applicazioni, come meglio precisato nel prospetto che costituisce parte integrante del presente verbale (Allegato A).

Per quanto riguarda, invece, la prova relativa all'accertamento della conoscenza della lingua straniera, la Dott.ssa Saddi Alessandra, componente aggiunto della Commissione, stabilisce, in accordo con i membri di quest'ultima, di predisporre una prova unica per tutti i candidati presenti, consistente nella lettura e traduzione di un testo, allegato al presente verbale (Allegato B), relativo alla lingua inglese.

Al fine dell'espletamento delle prove predette sono predisposte due apposite postazioni, con l'occorrenza necessario, all'interno dell'aula riservata alla prova orale.

Alle ore 10,00 il Segretario della Commissione, Dott. Andrea Madeddu, con l'ausilio del personale di assistenza (Dott. Andrea Madeddu), dà inizio all'accesso dei candidati all'area concorsuale.

I candidati effettuano il riconoscimento attraverso l'esibizione di un documento personale di identità in corso di validità.

I candidati esibiscono e consegnano, altresì, l'apposita autocertificazione con la quale attestano di non essere sottoposti alla misura dell'isolamento come misura di prevenzione della diffusione del contagio da COVID 19, di essere a conoscenza delle misure del contenimento del contagio vigenti alla data odierna e di aver rispettato le disposizioni emanate dalle Autorità competenti quali distanziamento sociale, utilizzo mascherine ed altro.

La Commissione comunica la necessità, per i candidati, di indossare obbligatoriamente, dal momento dell'accesso all'area concorsuale sino a quello dell'uscita, il dispositivo individuale di protezione delle vie aeree (mascherina), che, ove richiesto dagli interessati, è messo a disposizione dall'Azienda organizzatrice.

I candidati vengono fatti accomodare nelle apposite postazioni operative adeguatamente distanziati l'uno dall'altro.

Si procede, dunque, all'appello nominale ed alla registrazione dei presenti e degli assenti, come di seguito specificato:

NOMINATIVO	NATO IL	PRESENTE
CONGIU SIMONE	15/04/1980	Si
DERIU GIANFRANCO	14/10/1985	Si
GUASTINI ROBERTO	24/05/1968	Si
LODI FLAVIA CARINA	19/12/1974	Si
MANCA ROBERTO	03/02/1981	Si
PILIA TOMAS	16/10/1973	Si
PORCEDDU ROBERTO	15/05/1973	Si
PUDDU MASSIMO	11/02/1972	Si
RISTORI MARCO	04/07/1979	Si
SASSU ALESSANDRO	05/11/1984	Si
TORRACO NICOLA	27/03/1976	Si
TRUDU ADRIANO	23/04/1970	Si
URAS MARCO	01/04/1987	Si

Il Presidente della Commissione spiega ai candidati le modalità di espletamento della prova orale, precisando che la stessa si svolge in locale aperto al pubblico e che, pertanto, chiunque può assistervi.

I candidati sono introdotti singolarmente nel locale d'esame per essere sottoposti alla prova orale. Al fine di procedere all'espletamento della prova, alla presenza di tutti i candidati e con il consenso degli stessi, si effettua in modo casuale ed in modalità telematica l'estrazione della lettera alfabetica. Viene estratta la lettera C.

Si inizia, pertanto, dal candidato Congiu Simone e la prova prosegue seguendo l'ordine alfabetico. Il risultato della valutazione dei titoli è comunicato a ciascun candidato prima dell'effettuazione della prova orale che si svolge, per tutta la sua durata, alla presenza della Commissione, dell'esaminando e degli altri candidati presenti nell'aula in qualità di testimoni.

Ciascun candidato estrae la busta contenente la domanda relativa al profilo professionale a concorso, ne dà lettura, la sottoscrive e discute l'argomento assegnato.

Ultimata la discussione, ciascun candidato si sottopone alla prova di lingua ed alla prova informatica.

La prova orale si svolge con le modalità descritte per ogni singolo candidato.

Alle ore 13,00 tutti i candidati hanno regolarmente effettuato la prova.

Dopo breve discussione, a ciascun candidato è attribuito dalla Commissione, collegialmente e con voto palese, il seguente punteggio espresso in /20:

NOMINATIVO	NATO IL	DOMANDA ESTRATTA	VOTO PROVA ORALE/20	IDONEO/NON IDONEO
CONGIU SIMONE	15/04/1980	5	14,000	IDONEO
DERIU GIANFRANCO	14/10/1985	3	16,000	IDONEO
GUASTINI ROBERTO	24/05/1968	2	18,000	IDONEO
LODI FLAVIA CARINA	19/12/1974	11	20,000	IDONEO
MANCA ROBERTO	03/02/1981	6	14,000	IDONEO
PILIA TOMAS	16/10/1973	7	17,000	IDONEO
PORCEDDU ROBERTO	15/05/1973	13	14,000	IDONEO
PUDDU MASSIMO	11/02/1972	8	19,000	IDONEO
RISTORI MARCO	04/07/1979	12	16,000	IDONEO
SASSU ALESSANDRO	05/11/1984	14	16,000	IDONEO
TORRACO NICOLA	27/03/1976	9	15,000	IDONEO

De Riu *ED* *S* *in piano* *per*

TRUDU ADRIANO	23/04/1970	4	15,000	IDONEO
URAS MARCO	01/04/1987	1	18,000	IDONEO

Tutti i candidati presenti hanno conseguito l'idoneità nella prova di lingua inglese e di informatica. I risultati della prova orale saranno pubblicati sul sito internet aziendale dell'ARES Sardegna. La Commissione redige, pertanto, la seguente graduatoria di merito dei candidati, sulla base del punteggio complessivo determinato sommando quello conseguente alla valutazione dei titoli ai voti conseguiti nelle prove scritta, pratica ed orale:

Pos.	Cognome	Nome	Data nascita	Titoli	Prova scritta	Prova pratica	Prova orale	Totale
1	SASSU	ALESSANDRO	05/11/1984	0,818	28,000	20,000	16,000	64,818
2	URAS	MARCO	01/04/1987	1,130	29,000	15,000	18,000	63,130
3	TRUDU	ADRIANO	23/04/1970	5,321	28,000	14,000	15,000	62,321
4	CONGIU	SIMONE	15/04/1980	2,593	30,000	15,000	14,000	61,593
5	LODI	FLAVIA CARINA	19/12/1974	0,259	22,000	19,000	20,000	61,259
6	RISTORI	MARCO	04/07/1979	4,416	21,000	19,000	16,000	60,416
7	PILIA	TOMAS	16/10/1973	0,320	29,000	14,000	17,000	60,320
8	DERIU	GIANFRANCO	14/10/1985	1,288	25,000	18,000	16,000	60,288
9	PUDDU	MASSIMO	11/02/1972	1,100	22,000	17,000	19,000	59,100
10	GUASTINI	ROBERTO	24/05/1968	0,200	23,000	17,000	18,000	58,200
11	TORRACO	NICOLA	27/03/1976	1,177	21,000	15,000	15,000	52,177
12	PORCEDDU	ROBERTO	15/05/1973	0,200	23,000	14,000	14,000	51,200
13	MANCA	ROBERTO	03/02/1981	0,320	22,000	14,000	14,000	50,320

Terminati i lavori, la Commissione trasmette il presente verbale, nonché tutti gli atti del concorso al Direttore della SC Ricerca e Selezione Risorse Umane per i provvedimenti di competenza. La seduta si chiude alle ore 14,00.

Il presente verbale, letto e confermato, viene sottoscritto come segue:

Presidente: Ing. Galisai Marco



Componente: Ing. Testoni Giampiero



Componente: Ing. Rossi Michele



Componente aggiunto: Dott. Deplano Emiliano

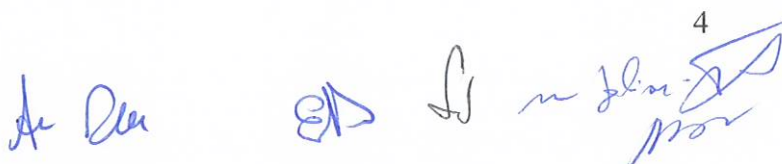


Componente aggiunto: Dott.ssa Saddi Alessandra



Segretario: Dott. Madeddu Andrea





Pubblico Concorso, per titoli ed esami, per la copertura a tempo indeterminato di n. 5 posti di Collaboratore Tecnico Professionale - Ingegnere Elettronico, Cat. D

Accertamento della conoscenza dell'uso delle apparecchiature e delle applicazioni informatiche più diffuse

Traccia 1

1. All'interno del file "Prova1.xlsx":

- a. Inserire le formule necessarie per il calcolo dell' **"Importo Fattura IVA"** con riferimento assoluto a cella ove presente percentuale IVA pre-impostata.

Id fatt.	Fornitore	Importo Fattura	Importo Fattura IVA	Tipologia Assistenza	Trimestre Competenza
1	Ditta1	€ 9.855,00		Ordinaria	1
4	Ditta1	€ 9.855,00		Ordinaria	2
5	Ditta1	€ 2.390,00		A richiesta	2
6	Ditta1	€ 9.855,00		Ordinaria	3
9	Ditta1	€ 9.855,00		Ordinaria	4
12	Ditta1	€ 4.000,00		A richiesta	4
3	Ditta2	€ 7.880,00		Ordinaria	1
12	Ditta2	€ 7.880,00		Ordinaria	2
63	Ditta2	€ 7.880,00		Ordinaria	3
68	Ditta2	€ 7.880,00		Ordinaria	4
69	Ditta2	€ 1.200,00		A richiesta	4
3	Ditta3	€ 11.030,00		Ordinaria	1
8	Ditta3	€ 11.030,00		Ordinaria	2
32	Ditta3	€ 11.030,00		Ordinaria	3
38	Ditta3	€ 11.030,00		Ordinaria	4
6	Ditta4	€ 8.289,00		Ordinaria	1
7	Ditta4	€ 4.800,00		A richiesta	1
9	Ditta4	€ 8.289,00		Ordinaria	2
12	Ditta4	€ 5.600,00		A richiesta	2
13	Ditta4	€ 1.200,00		A richiesta	2
15	Ditta4	€ 8.289,00		Ordinaria	3
31	Ditta4	€ 8.289,00		Ordinaria	4

2. Con riferimento alla tabella completa del punto 1:

- a. Inserire una "Tabella pivot" che rappresenti per colonna il **Trimestre Competenza** e per riga il **Fornitore** e i valori **Importo Fattura IVA** relativi alle singole fatture, distinti per **Tipologia Assistenza**.
- b. Escludere dalla visualizzazione il **Trimestre Competenza** numero 1.

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Id fatt.	Fornitore	Importo Fattura	Importo Fattura IVA	Tipologia Assistenza	Trimestre Competenza
1	Ditta1	€ 9.855,00		Ordinaria	1
4	Ditta1	€ 9.855,00		Ordinaria	2
5	Ditta1	€ 2.390,00		A richiesta	2
6	Ditta1	€ 9.855,00		Ordinaria	3
9	Ditta1	€ 9.855,00		Ordinaria	4
12	Ditta1	€ 4.000,00		A richiesta	4
3	Ditta2	€ 7.880,00		Ordinaria	1
12	Ditta2	€ 7.880,00		Ordinaria	2
63	Ditta2	€ 7.880,00		Ordinaria	3
68	Ditta2	€ 7.880,00		Ordinaria	4
69	Ditta2	€ 1.200,00		A richiesta	4
3	Ditta3	€ 11.030,00		Ordinaria	1
8	Ditta3	€ 11.030,00		Ordinaria	2
32	Ditta3	€ 11.030,00		Ordinaria	3
38	Ditta3	€ 11.030,00		Ordinaria	4
6	Ditta4	€ 8.289,00		Ordinaria	1
7	Ditta4	€ 4.800,00		A richiesta	1
9	Ditta4	€ 8.289,00		Ordinaria	2
12	Ditta4	€ 5.600,00		A richiesta	2
13	Ditta4	€ 1.200,00		A richiesta	2
15	Ditta4	€ 8.289,00		Ordinaria	3
31	Ditta4	€ 8.289,00		Ordinaria	4



Random-access memory

From Wikipedia, the free encyclopedia

Random-access memory (**RAM**; /ræm/) is a form of computer memory that can be read and changed in any order, typically used to store working data and machine code.^{[1][2]} A random-access memory device allows data items to be read or written in almost the same amount of time irrespective of the physical location of data inside the memory, in contrast with other direct-access data storage media (such as hard disks, CD-RWs, DVD-RWs and the older magnetic tapes and drum memory), where the time required to read and write data items varies significantly depending on their physical locations on the recording medium, due to mechanical limitations such as media rotation speeds and arm movement.

RAM contains multiplexing and demultiplexing circuitry, to connect the data lines to the addressed storage for reading or writing the entry. Usually more than one bit of storage is accessed by the same address, and RAM devices often have multiple data lines and are said to be "8-bit" or "16-bit", etc. devices.^[clarification needed]

In today's technology, random-access memory takes the form of integrated circuit (IC) chips with MOS (metal-oxide-semiconductor) memory cells. RAM is normally associated with volatile types of memory (such as dynamic random-access memory (DRAM) modules), where stored information is lost if power is removed, although non-volatile RAM has also been developed.^[3] Other types of non-volatile memories exist that allow random access for read operations, but either do not allow write operations or have other kinds of limitations on them. These include most types of ROM and a type of flash memory called *NOR-Flash*.

The two main types of volatile random-access semiconductor memory are static random-access memory (SRAM) and dynamic random-access memory (DRAM). Commercial uses of semiconductor RAM date back to 1965, when IBM introduced the SP95 SRAM chip for their System/360 Model 95 computer, and Toshiba used DRAM memory cells for its Toscal BC-1411 electronic calculator, both based on bipolar transistors. Commercial MOS memory, based on MOS transistors, was developed in the late 1960s, and has since been the basis for all commercial semiconductor memory. The first commercial DRAM IC chip, the Intel 1103, was introduced in October 1970. Synchronous dynamic random-access memory (SDRAM) later debuted with the Samsung KM48SL2000 chip in 1992.^[4]

Early computers used relays, mechanical counters^[4] or delay lines for main memory functions. Ultrasonic delay lines were serial devices which could only reproduce data in the order it was written. Drum memory could be expanded at relatively low cost but efficient retrieval of memory items required knowledge of the physical layout of the drum to optimize speed. Latches built out of vacuum tube triodes, and later, out of discrete transistors, were used for smaller and faster memories such as registers. Such registers were relatively large and too costly to use for large amounts of data; generally only a few dozen or few hundred bits of such memory could be provided.

The first practical form of random-access memory was the Williams tube starting in 1947. It stored data as electrically charged spots on the face of a cathode-ray tube. Since the electron beam of the CRT could read and write the spots on the tube in any order, memory was random access. The capacity of the Williams tube was a few hundred to around a thousand bits, but it was much smaller, faster, and more power-efficient than using individual vacuum tube latches. Developed at the University of Manchester in England, the Williams tube provided the medium on which the first electronically stored program was implemented in

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the Manchester Baby computer, which first successfully ran a program on 21 June 1948.^[5] In fact, rather than the Williams tube memory being designed for the Baby, the Baby was a testbed to demonstrate the reliability of the memory.^{[6][7]}

Magnetic-core memory was invented in 1947 and developed up until the mid-1970s. It became a widespread form of random-access memory, relying on an array of magnetized rings. By changing the sense of each ring's magnetization, data could be stored with one bit stored per ring. Since every ring had a combination of address wires to select and read or write it, access to any memory location in any sequence was possible. Magnetic core memory was the standard form of computer memory system until displaced by solid-state MOS (metal-oxide-silicon) semiconductor memory in integrated circuits (ICs) during the early 1970s.^[8]

Prior to the development of integrated read-only memory (ROM) circuits, *permanent* (or *read-only*) random-access memory was often constructed using diode matrices driven by address decoders, or specially wound core rope memory planes.^[citation needed]

Semiconductor memory began in the 1960s with bipolar memory, which used bipolar transistors. While it improved performance, it could not compete with the lower price of magnetic core memory.^[9]

MOS RAM

The invention of the MOSFET (metal-oxide-semiconductor field-effect transistor), also known as the MOS transistor, by Mohamed M. Atalla and Dawon Kahng at Bell Labs in 1959,^[10] led to the development of metal-oxide-semiconductor (MOS) memory by John Schmidt at Fairchild Semiconductor in 1964.^{[8][11]} In addition to higher performance, MOS semiconductor memory was cheaper and consumed less power than magnetic core memory.^[8] The development of silicon-gate MOS integrated circuit (MOS IC) technology by Federico Faggin at Fairchild in 1968 enabled the production of MOS memory chips.^[12] MOS memory overtook magnetic core memory as the dominant memory technology in the early 1970s.^[8]

An integrated bipolar static random-access memory (SRAM) was invented by Robert H. Norman at Fairchild Semiconductor in 1963.^[13] It was followed by the development of MOS SRAM by John Schmidt at Fairchild in 1964.^[8] SRAM became an alternative to magnetic-core memory, but required six MOS transistors for each bit of data.^[14] Commercial use of SRAM began in 1965, when IBM introduced the SP95 memory chip for the System/360 Model 95.^[9]

Dynamic random-access memory (DRAM) allowed replacement of a 4 or 6-transistor latch circuit by a single transistor for each memory bit, greatly increasing memory density at the cost of volatility. Data was stored in the tiny capacitance of each transistor, and had to be periodically refreshed every few milliseconds before the charge could leak away. Toshiba's Toscal BC-1411 electronic calculator, which was introduced in 1965,^{[15][16][17]} used a form of capacitive bipolar DRAM, storing 180-bit data on discrete memory cells, consisting of germanium bipolar transistors and capacitors.^{[16][17]} While it offered improved performance over magnetic-core memory, bipolar DRAM could not compete with the lower price of the then dominant magnetic-core memory.^[18]

MOS technology is the basis for modern DRAM. In 1966, Dr. Robert H. Dennard at the IBM Thomas J. Watson Research Center was working on MOS memory. While examining the characteristics of MOS technology, he found it was capable of building capacitors, and that storing a charge or no charge on the MOS capacitor could represent the 1 and 0 of a bit, while the MOS transistor could control writing the charge to the capacitor. This led to his development of a single-transistor DRAM memory cell.^[14] In 1967, Dennard filed a patent

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under IBM for a single-transistor DRAM memory cell, based on MOS technology.^[19] The first commercial DRAM IC chip was the Intel 1103, which was manufactured on an 8 μm MOS process with a capacity of 1 kbit, and was released in 1970.^{[8][20][21]}

Synchronous dynamic random-access memory (SDRAM) was developed by Samsung Electronics. The first commercial SDRAM chip was the Samsung KM48SL2000, which had a capacity of 16 Mbit.^[22] It was introduced by Samsung in 1992,^[23] and mass-produced in 1993.^[22] The first commercial DDR SDRAM (double data rate SDRAM) memory chip was Samsung's 64 Mbit DDR SDRAM chip, released in June 1998.^[24] GDDR (graphics DDR) is a form of DDR SGRAM (synchronous graphics RAM), which was first released by Samsung as a 16 Mbit memory chip in 1998.^[25]

Types

The two widely used forms of modern RAM are static RAM (SRAM) and dynamic RAM (DRAM). In SRAM, a bit of data is stored using the state of a six-transistor memory cell, typically using six MOSFETs (metal-oxide-semiconductor field-effect transistors). This form of RAM is more expensive to produce, but is generally faster and requires less dynamic power than DRAM. In modern computers, SRAM is often used as cache memory for the CPU. DRAM stores a bit of data using a transistor and capacitor pair (typically a MOSFET and MOS capacitor, respectively),^[26] which together comprise a DRAM cell. The capacitor holds a high or low charge (1 or 0, respectively), and the transistor acts as a switch that lets the control circuitry on the chip read the capacitor's state of charge or change it. As this form of memory is less expensive to produce than static RAM, it is the predominant form of computer memory used in modern computers.

Both static and dynamic RAM are considered *volatile*, as their state is lost or reset when power is removed from the system. By contrast, read-only memory (ROM) stores data by permanently enabling or disabling selected transistors, such that the memory cannot be altered. Writeable variants of ROM (such as EEPROM and NOR flash) share properties of both ROM and RAM, enabling data to persist without power and to be updated without requiring special equipment. ECC memory (which can be either SRAM or DRAM) includes special circuitry to detect and/or correct random faults (memory errors) in the stored data, using parity bits or error correction codes.

In general, the term *RAM* refers solely to solid-state memory devices (either DRAM or SRAM), and more specifically the main memory in most computers. In optical storage, the term DVD-RAM is somewhat of a misnomer since, unlike CD-RW or DVD-RW it does not need to be erased before reuse. Nevertheless, a DVD-RAM behaves much like a hard disc drive if somewhat slower.

Memory cell

Main article: Memory cell (computing)

The memory cell is the fundamental building block of computer memory. The memory cell is an electronic circuit that stores one bit of binary information and it must be set to store a logic 1 (high voltage level) and reset to store a logic 0 (low voltage level). Its value is maintained/stored until it is changed by the set/reset process. The value in the memory cell can be accessed by reading it.

In SRAM, the memory cell is a type of flip-flop circuit, usually implemented using FETs. This means that SRAM requires very low power when not being accessed, but it is expensive and has low storage density.

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A second type, DRAM, is based around a capacitor. Charging and discharging this capacitor can store a "1" or a "0" in the cell. However, the charge in this capacitor slowly leaks away, and must be refreshed periodically. Because of this refresh process, DRAM uses more power, but it can achieve greater storage densities and lower unit costs compared to SRAM.

Addressing

To be useful, memory cells must be readable and writeable. Within the RAM device, multiplexing and demultiplexing circuitry is used to select memory cells. Typically, a RAM device has a set of address lines A0... An, and for each combination of bits that may be applied to these lines, a set of memory cells are activated. Due to this addressing, RAM devices virtually always have a memory capacity that is a power of two.

Usually several memory cells share the same address. For example, a 4 bit 'wide' RAM chip has 4 memory cells for each address. Often the width of the memory and that of the microprocessor are different, for a 32 bit microprocessor, eight 4 bit RAM chips would be needed.

Often more addresses are needed than can be provided by a device. In that case, external multiplexors to the device are used to activate the correct device that is being accessed.

Memory hierarchy

Main article: Memory hierarchy

One can read and over-write data in RAM. Many computer systems have a memory hierarchy consisting of processor registers, on-die SRAM caches, external caches, DRAM, paging systems and virtual memory or swap space on a hard drive. This entire pool of memory may be referred to as "RAM" by many developers, even though the various subsystems can have very different access times, violating the original concept behind the *random access* term in RAM. Even within a hierarchy level such as DRAM, the specific row, column, bank, rank, channel, or interleave organization of the components make the access time variable, although not to the extent that access time to rotating storage media or a tape is variable. The overall goal of using a memory hierarchy is to obtain the highest possible average access performance while minimizing the total cost of the entire memory system (generally, the memory hierarchy follows the access time with the fast CPU registers at the top and the slow hard drive at the bottom).

In many modern personal computers, the RAM comes in an easily upgraded form of modules called memory modules or DRAM modules about the size of a few sticks of chewing gum. These can quickly be replaced should they become damaged or when changing needs demand more storage capacity. As suggested above, smaller amounts of RAM (mostly SRAM) are also integrated in the CPU and other ICs on the motherboard, as well as in hard-drives, CD-ROMs, and several other parts of the computer system.

Other uses of RAM

In addition to serving as temporary storage and working space for the operating system and applications, RAM is used in numerous other ways.

Virtual memory

Main article: Virtual memory

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Most modern operating systems employ a method of extending RAM capacity, known as "virtual memory". A portion of the computer's hard drive is set aside for a *paging file* or a *scratch partition*, and the combination of physical RAM and the paging file form the system's total memory. (For example, if a computer has 2 GB (1024^3 B) of RAM and a 1 GB page file, the operating system has 3 GB total memory available to it.) When the system runs low on physical memory, it can "swap" portions of RAM to the paging file to make room for new data, as well as to read previously swapped information back into RAM. Excessive use of this mechanism results in thrashing and generally hampers overall system performance, mainly because hard drives are far slower than RAM.

RAM disk

Main article: RAM drive

Software can "partition" a portion of a computer's RAM, allowing it to act as a much faster hard drive that is called a RAM disk. A RAM disk loses the stored data when the computer is shut down, unless memory is arranged to have a standby battery source, or changes to the RAM disk are written out to a nonvolatile disk. The RAM disk is reloaded from the physical disk upon RAM disk initialization.

Shadow RAM

Sometimes, the contents of a relatively slow ROM chip are copied to read/write memory to allow for shorter access times. The ROM chip is then disabled while the initialized memory locations are switched in on the same block of addresses (often write-protected). This process, sometimes called *shadowing*, is fairly common in both computers and embedded systems.

As a common example, the BIOS in typical personal computers often has an option called "use shadow BIOS" or similar. When enabled, functions that rely on data from the BIOS's ROM instead use DRAM locations (most can also toggle shadowing of video card ROM or other ROM sections). Depending on the system, this may not result in increased performance, and may cause incompatibilities. For example, some hardware may be inaccessible to the operating system if shadow RAM is used. On some systems the benefit may be hypothetical because the BIOS is not used after booting in favor of direct hardware access. Free memory is reduced by the size of the shadowed ROMs.^[27]

Recent developments

Several new types of non-volatile RAM, which preserve data while powered down, are under development. The technologies used include carbon nanotubes and approaches utilizing Tunnel magnetoresistance. Amongst the 1st generation MRAM, a 128 kbit (128×2^{10} bytes) chip was manufactured with 0.18 μm technology in the summer of 2003.^[citation needed] In June 2004, Infineon Technologies unveiled a 16 MB (16×2^{20} bytes) prototype again based on 0.18 μm technology. There are two 2nd generation techniques currently in development: thermal-assisted switching (TAS)^[28] which is being developed by Crocus Technology, and spin-transfer torque (STT) on which Crocus, Hynix, IBM, and several other companies are working.^[29] Nantero built a functioning carbon nanotube memory prototype 10 GB (10×2^{30} bytes) array in 2004. Whether some of these technologies can eventually take significant market share from either DRAM, SRAM, or flash-memory technology, however, remains to be seen.

Since 2006, "solid-state drives" (based on flash memory) with capacities exceeding 256 gigabytes and performance far exceeding traditional disks have become available. This

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development has started to blur the definition between traditional random-access memory and "disks", dramatically reducing the difference in performance.

Some kinds of random-access memory, such as "EcoRAM", are specifically designed for server farms, where low power consumption is more important than speed.^[30]

Memory wall

The "memory wall" is the growing disparity of speed between CPU and memory outside the CPU chip. An important reason for this disparity is the limited communication bandwidth beyond chip boundaries, which is also referred to as *bandwidth wall*. From 1986 to 2000, CPU speed improved at an annual rate of 55% while memory speed only improved at 10%. Given these trends, it was expected that memory latency would become an overwhelming bottleneck in computer performance.^[31]

CPU speed improvements slowed significantly partly due to major physical barriers and partly because current CPU designs have already hit the memory wall in some sense. Intel summarized these causes in a 2005 document.^[32]

First of all, as chip geometries shrink and clock frequencies rise, the transistor leakage current increases, leading to excess power consumption and heat... Secondly, the advantages of higher clock speeds are in part negated by memory latency, since memory access times have not been able to keep pace with increasing clock frequencies. Third, for certain applications, traditional serial architectures are becoming less efficient as processors get faster (due to the so-called Von Neumann bottleneck), further undercutting any gains that frequency increases might otherwise buy. In addition, partly due to limitations in the means of producing inductance within solid state devices, resistance-capacitance (RC) delays in signal transmission are growing as feature sizes shrink, imposing an additional bottleneck that frequency increases don't address.

The RC delays in signal transmission were also noted in "Clock Rate versus IPC: The End of the Road for Conventional Microarchitectures"^[33] which projected a maximum of 12.5% average annual CPU performance improvement between 2000 and 2014.

A different concept is the processor-memory performance gap, which can be addressed by 3D integrated circuits that reduce the distance between the logic and memory aspects that are further apart in a 2D chip.^[34] Memory subsystem design requires a focus on the gap, which is widening over time.^[35] The main method of bridging the gap is the use of caches; small amounts of high-speed memory that houses recent operations and instructions nearby the processor, speeding up the execution of those operations or instructions in cases where they are called upon frequently. Multiple levels of caching have been developed to deal with the widening gap, and the performance of high-speed modern computers relies on evolving caching techniques.^[36] There can be up to a 53% difference between the growth in speed of processor and the lagging speed of main memory access.^[37]

Solid-state hard drives have continued to increase in speed, from ~400 Mbit/s via SATA3 in 2012 up to ~3 GB/s via NVMe/PCIe in 2018, closing the gap between RAM and hard disk speeds, although RAM continues to be an order of magnitude faster, with single-lane DDR4 3200 capable of 25 GB/s, and modern GDDR even faster. Fast, cheap, non-volatile solid state drives have replaced some functions formerly performed by RAM, such as holding certain data for immediate availability in server farms - 1 terabyte of SSD storage can be had for \$200, while 1 TB of RAM would cost thousands of dollars.^{[38][39]}

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